

REMARKS

Claims 1-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA), in view of Schilling et al., Electronic Circuits: Discrete and Integrated, 1979, pages 560-615.

In the AAPA, the input pattern set in the scan cells as a test pattern for the internal circuit of the LSI is a fixed pattern, and the output buffers sequentially receive and output the data without simultaneously changing among the output buffers by use of the delay elements inserted between the scan cells and the output buffers. Schilling et al. teaches noise margin and fan-out requirements on logic gates.

In contrast, the present invention relates to a method to generate the input pattern set in the scan cells as a test pattern for the internal circuit of the LSI, the test pattern preventing a noise problem. The AAPA fails to teach or suggest a method to generate an input pattern for the internal circuit set in the scan cells. Schilling et al. teaches only noise margin and fan-out requirements, these requirements being for the internal circuit (a logical circuit) of the LSI, and Schilling et al. does not teach noise values generated by output buffers.

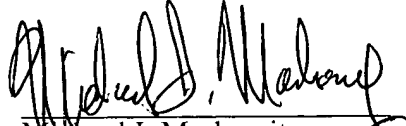
CLOSING

In view of the above amendments, it is believed that independent claims 1, 2, and 4 are in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on
Deposit Account 50-1290.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read "Michael I. Markowitz", written over a horizontal line.

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